

P-Channel NexFET™ Power MOSFET

Check for Samples: [CSD25213W10](#)

FEATURES

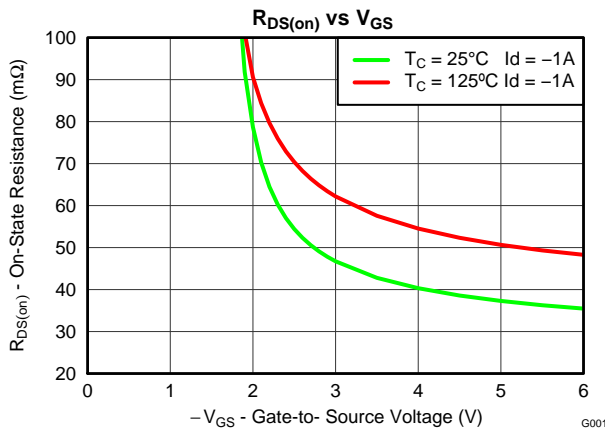
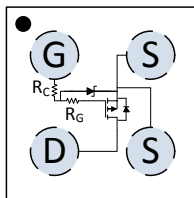
- Ultra Low Qg and Qgd
- Small Footprint 1mm x 1mm
- Low Profile 0.62mm Height
- Pb Free
- Gate-Source Voltage Clamp
- Gate ESD Protection
- RoHS Compliant
- Halogen Free

APPLICATIONS

- Battery Management
- Load Switch
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

Top View


PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	-20	V
Q_g	Gate Charge Total (4.5V)	2.2	nC
Q_{gd}	Gate Charge Gate to Drain	0.14	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -2.5V$	54 mΩ
		$V_{GS} = -4.5V$	39 mΩ
$V_{GS(th)}$	Threshold Voltage	-0.85	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD25213W10	1 x 1 Wafer Level Package	7-inch reel	3000	Tape and Reel

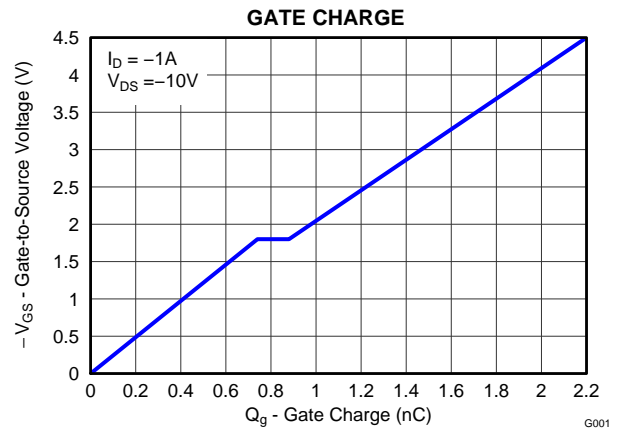
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	-6.0	V
I_D	Continuous Drain Current, $T_A = 25^\circ\text{C}^{(1)}$	-1.6	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}^{(2)}$	-16	A
I_G	Continuous Gate Clamp Current ⁽³⁾	-5	mA
P_D	Power Dissipation ⁽¹⁾	1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

(1) $R_{\theta JA} = 75^\circ\text{C/W}$ on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

(3) Limited by gate resistance.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
BV_{GSS}	Gate to Source Voltage;	$V_{DS} = 0V, I_G = -250\mu A$	-6.0			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = -10V$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = -6V$			-100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.60	-0.85	-1.10	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -2.5V, I_D = -1A$		54	67	m Ω
		$V_{GS} = -4.5V, I_D = -1A$		39	47	m Ω
g_{fs}	Transconductance	$V_{DS} = -10V, I_D = -1A$		6.2		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = -10V, f = 10kHz$		368	478	pF
C_{OSS}	Output Capacitance			148	192	pF
C_{RSS}	Reverse Transfer Capacitance			7.8	10.1	pF
R_G	Series Gate Resistance			20		Ω
R_C	Series Clamp Resistance			5000		Ω
Q_g	Gate Charge Total (-4.5V)	$V_{DS} = -10V, I_D = -1A$		2.2	2.9	nC
Q_{gd}	Gate Charge Gate to Drain			0.14		nC
Q_{gs}	Gate Charge Gate to Source			0.74		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.43		nC
Q_{OSS}	Output Charge	$V_{DS} = -10V, V_{GS} = 0V$		2.5		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = -10V, V_{GS} = -2.5V, I_D = -1A$ $R_G = 10\Omega$		510		ns
t_r	Rise Time			520		ns
$t_{d(off)}$	Turn Off Delay Time			1000		ns
t_f	Fall Time			970		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_S = -1A, V_{GS} = 0V$		-0.77	-1	V
Q_{rr}	Reverse Recovery Charge	$V_{DS} = -10V, I_F = -1A,$ $di/dt = 200A/\mu s$		4.0		nC
t_{rr}	Reverse Recovery Time	$V_{DS} = -10V, I_F = -1A,$ $di/dt = 200A/\mu s$		11		ns

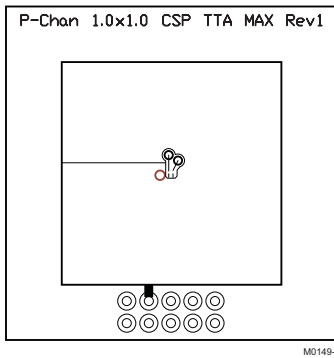
THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

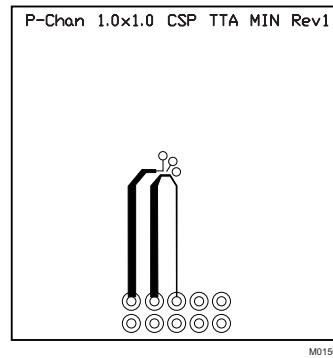
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to Ambient Thermal Resistance ⁽¹⁾		75		$^\circ\text{C}/\text{W}$
	Junction to Ambient Thermal Resistance ⁽²⁾		265		$^\circ\text{C}/\text{W}$

(1) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.



Max $R_{\theta JA} = 90^{\circ}\text{C/W}$
when mounted on
1 inch² of 2 oz. Cu.



Max $R_{\theta JA} = 333^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

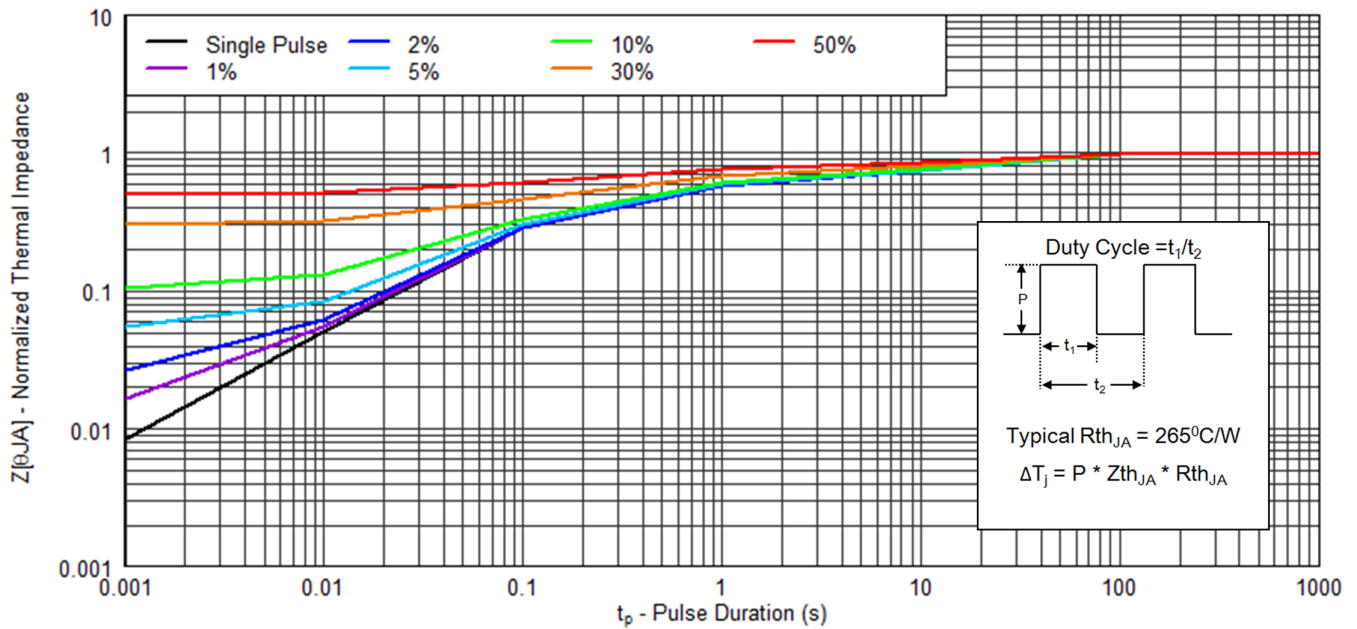


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

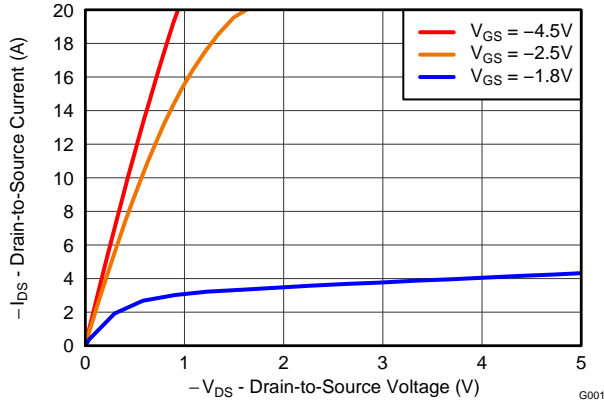


Figure 2. Saturation Characteristics

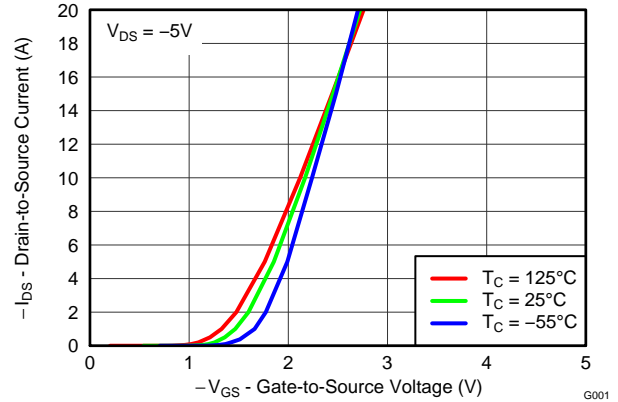


Figure 3. Transfer Characteristics

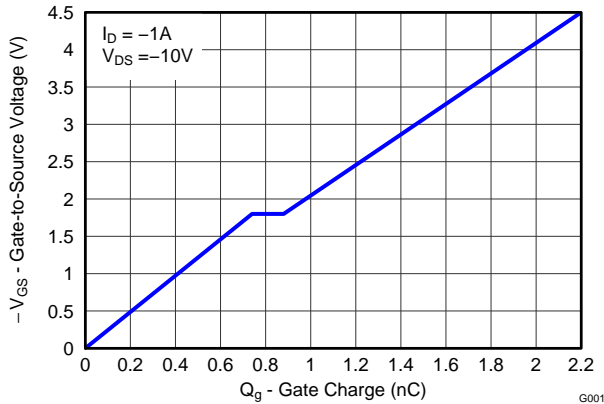


Figure 4. Gate Charge

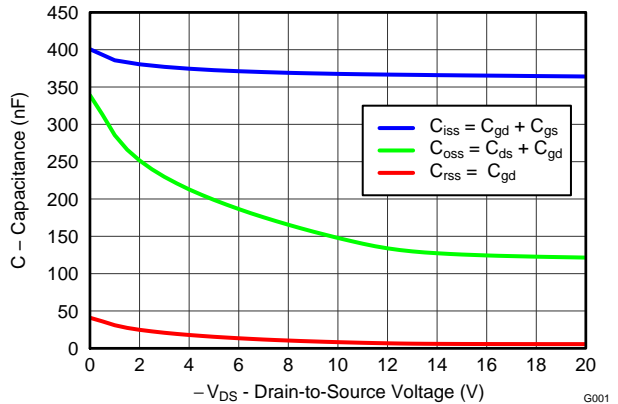


Figure 5. Capacitance

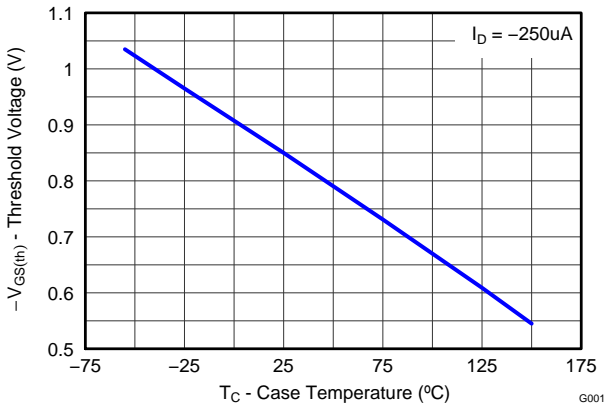


Figure 6. Threshold Voltage vs. Temperature

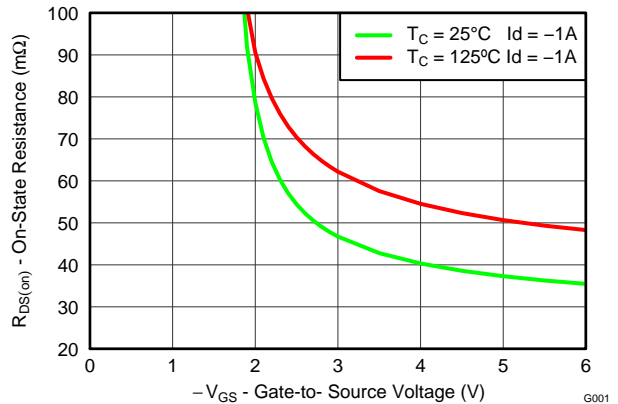


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

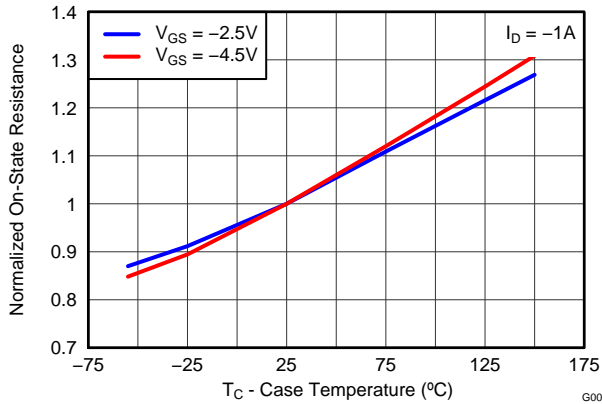


Figure 8. Normalized On-State Resistance vs. Temperature

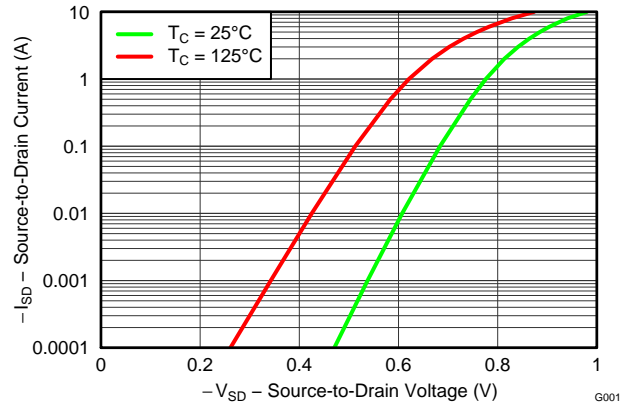


Figure 9. Typical Diode Forward Voltage

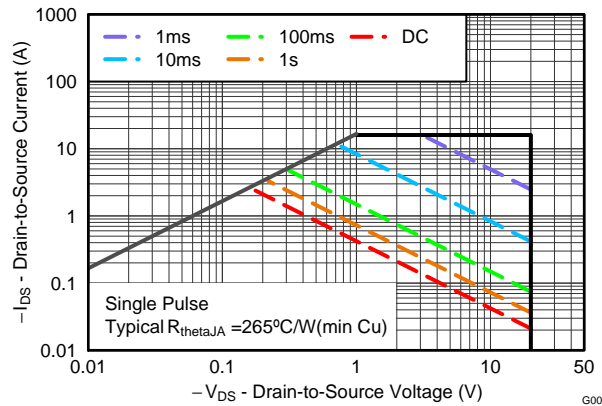


Figure 10. Maximum Safe Operating Area

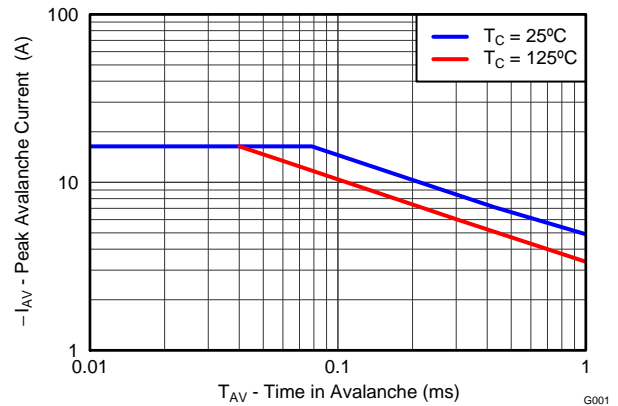


Figure 11. Single Pulse Unclamped Inductive Switching

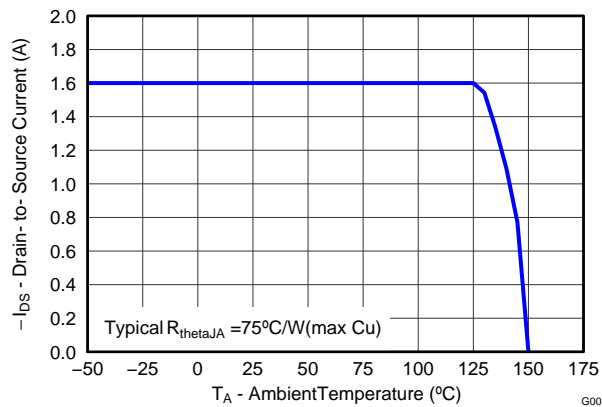
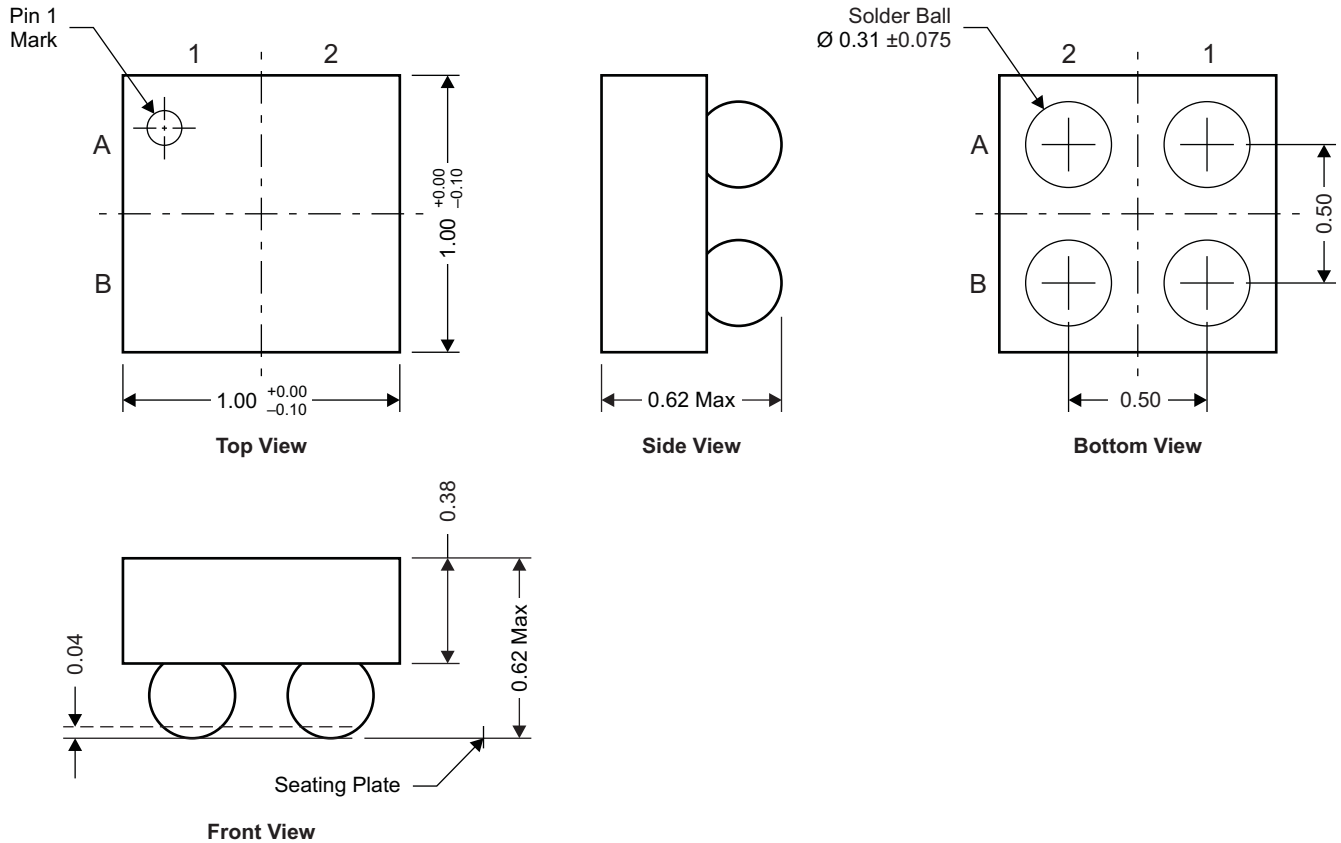


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD25213W10 Package Dimensions



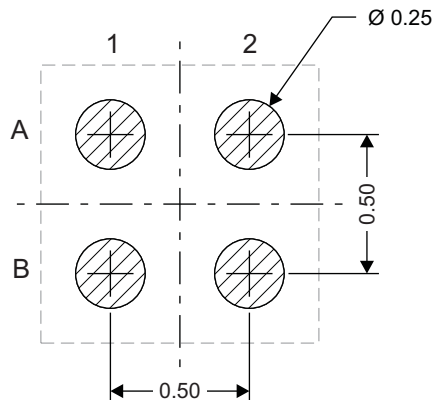
NOTE: All dimensions are in mm (unless otherwise specified)

M0151-01

Pin Configuration Table

POSITION	DESIGNATION
A1	Gate
B1	Drain
A2, B2	Source

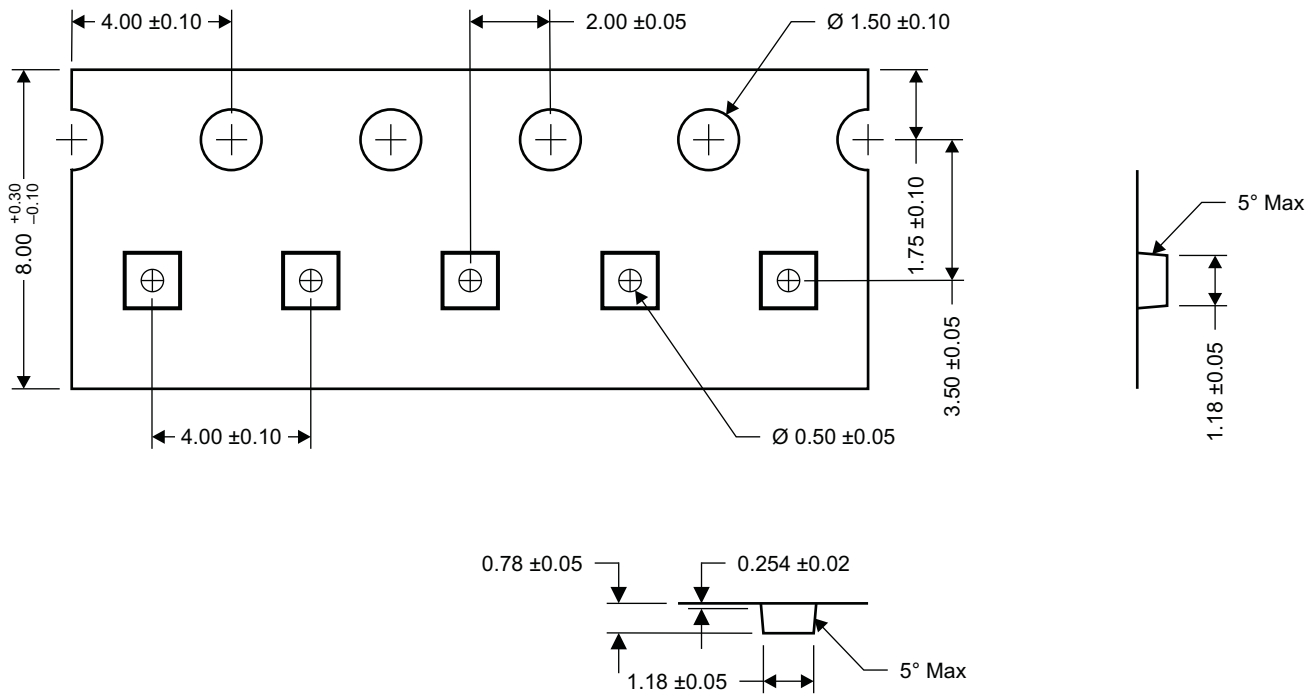
Land Pattern Recommendation



M0152-01

NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



- (1) All dimensions are in mm (unless otherwise specified)
- (2) Pin 1 will be oriented in the top left quadrant of the tape enclosure (closest to the carrier tape sprocket holes).

M0153-01

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25213W10	PREVIEW	DSBGA	YZB	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-55 to 150	213	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

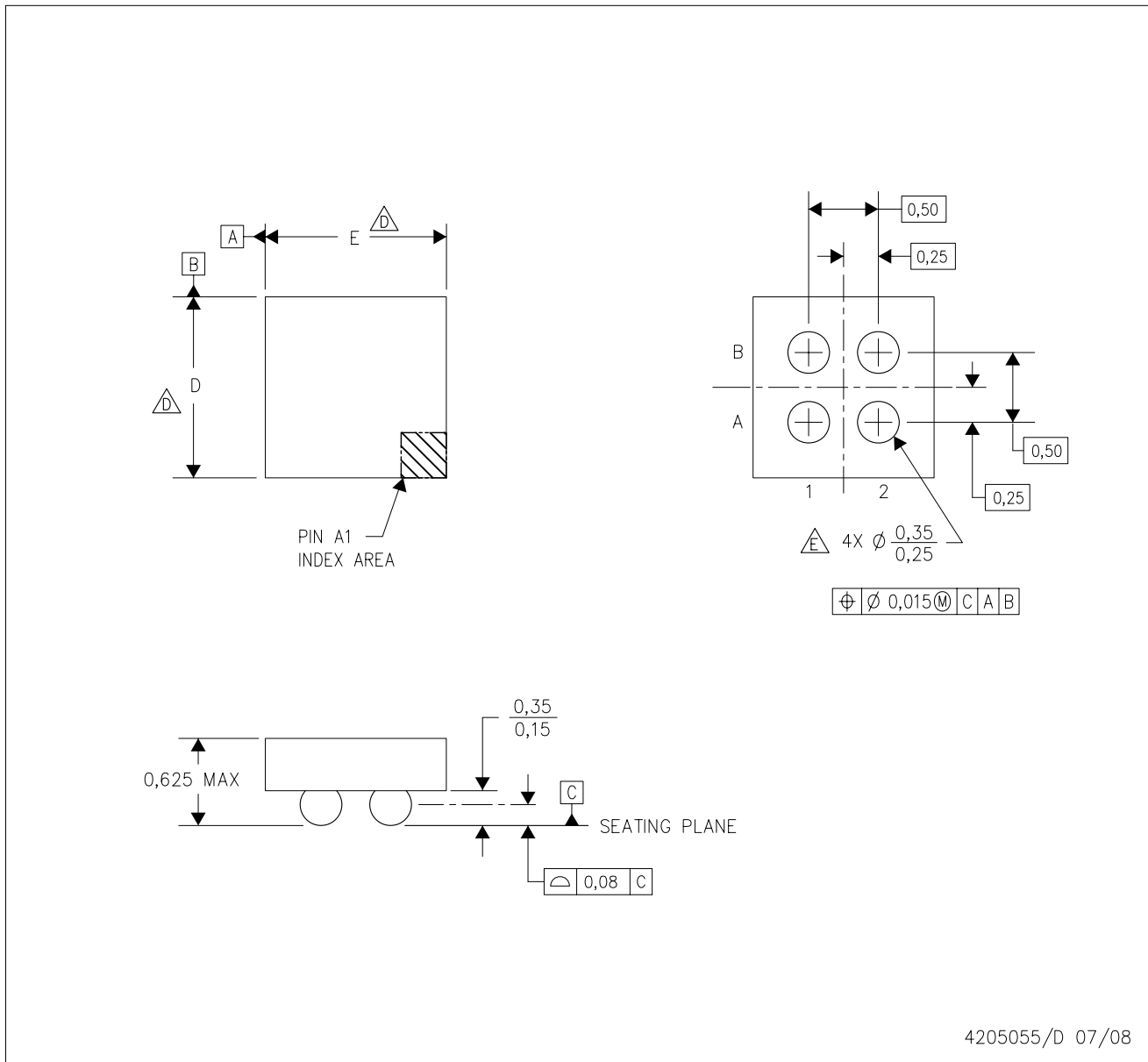
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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YZB (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



4205055/D 07/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - $\triangle D$ Devices in YZB package can have dimension D ranging from 0.94 to 1.65 mm and dimension E ranging from 0.94 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
2 x 2 matrix pattern is shown for illustration only.
 - F. This package contains lead-free balls.
Refer to YEB (Drawing #4204178) for tin-lead (SnPb) balls.

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